Reliability Challenges and Design Considerations for Wafer-Level Packages

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Abstract

Wafer-Level Packaging (WLP) is essentially a true chip-scale packaging (CSP) technology, since the resulting package is practically of the same size as the die. Furthermore, wafer-level packaging paves the way for true integration of wafer fab, packaging, test, and burn-in at wafer level, for the ultimate streamlining of the manufacturing process undergone by a device from silicon start to customer shipment. There are several WLP technology classifications. Redistribution Layer and Bump technology, the most widely-used WLP technology, extends the conventional wafer fab process with an additional step that deposits a multi-layer thin-film metal rerouting and interconnection system to each device on the wafer. In this paper, an overview of the state of art WLP packaging technologies will be presented. The emphasis will be given to the challenges in reliability and the solutions based on the design.

Introduction

Wafer-Level Packaging (WLP) is essentially a true chip-scale packaging (CSP) technology, since the resulting package is practically of the same size as the die [1-11]. Furthermore, wafer-level packaging paves the way for true integration of wafer fab, packaging, test, and burn-in at wafer level, for the ultimate streamlining of the manufacturing process undergone by a device from silicon start to customer shipment. There are four (4) WLP technology classifications: redistribution layer and bump technology, encapsulated copper post technology, encapsulated wire bond technology, and encapsulated beam lead technology [2]. Redistribution Layer and Bump technology, the most widely-used WLP technology, extends the conventional wafer fab process with an additional step that deposits a multi-layer thin-film metal rerouting and interconnection system to each device on the wafer. This is achieved using the same standard photolithography and thin film deposition techniques employed in the device fabrication itself. This additional level of interconnection redistributes the peripheral bonding pads of each chip to an area array of underbump metal (UBM) pads that are evenly deployed over the chip's surface. The solder balls or bumps used in connecting the device to the application circuit board are subsequently placed over these UBM pads. Aside from providing the WLP's means of external connection, this redistribution technique also improves chip reliability by allowing the use of larger and more robust balls for interconnection and better thermal management of the device's I/O system. Encapsulated Copper Post technology is very similar to redistribution and bump technology in the sense that the chip's bond pads are also rerouted into an area array of interconnection points. In this technology, however, these interconnection points are in the form of electroplated copper posts, instead of pads. These copper posts provide enough stand-off for the active wafer surface to be encapsulated in low-stress epoxy by transfer molding, exposing only the top portions of the posts where the solder balls will be attached.

In this paper, an overview of the state of art WLP packaging technologies will be presented. The emphasis will be given to discuss the challenges in reliability and the solutions based on the design.

Bump on Pad WLP

Bump on pad WLP is a traditional wafer level packaging technology and the process is very similar to a typical flip chip technology. One of those structures is the bump-on-nitride (BON) structure, consisting of solder bump and under bump metal (UBM) seated on the thin inorganic passivation as shown in Fig. 1.

The semiconductor devices utilizing BON WLPs are limited to 5x5 or less area arrays at 0.5mm pitch [5]. There are two reasons why traditional WLPs are predominately utilized by components with relatively low I/O counts. The first is related to die size. The smaller a given component is, the higher the associated die count per wafer. WLP technologies by their very nature result in a lower cost per die (vs. traditional wirebond) when the die count per wafer is high. The second reason is that the solder joint reliability of WLPs is limited compared to the other CSPs. As the number of I/O per die increases (and thus the Distance to Neutral Point increases), the WLP may not achieve prescribed solder joint reliability requirements. As wafer sizes continue to increase, the effective die size for WLPs to be cost-competitive also increases. To take advantage of this trend the solder joint reliability of WLPs needs to be improved.

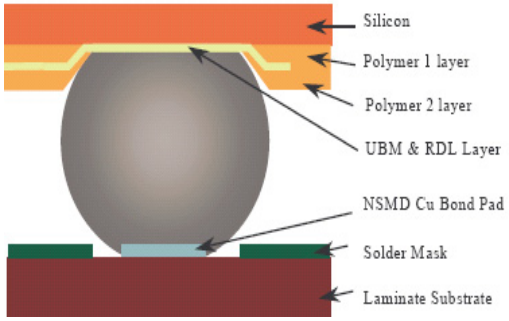

Fig. 1 Schematic diagram of BON structure WLP

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Cu Post WLP

Fig. 2 shows a schematic of Cu post WLP structure. The processes involving in making the Cu post is shown in Fig. 3 [6], peripheral pads on the wafer are rearranged in a real array pattern after photolithographic plating. Then metal posts about 100μm high are fabricated on the wafer. After encapsulating the entire surface of the wafer using the new encapsulation method, a package the same size as the chip is fabricated using a wafer-level packaging method. This method involves dividing the wafer into individual semiconductor packages by a standard dicing process. The detailed processes are described in the following,

1. The first step in the formation of posts and the rearrangement of pads is the formation of a polyimide cover film on a device wafer. This layer is a stress buffer against molding pressure. It also improves the adhesive properties between the wafer and the encapsulant. In the next step, the sputtering is applied to fabricate a thin metal film onto the surface of the wafer. The film consists of an adhesion metal layer and a conducting layer (copper in general). These thin metal films are the plating base used in the rerouting process and the metal post-forming process. After forming a patterned resist on the thin metal film surface, a redistribution trace is fabricated by electrolytic plating. After these processes, the resist is reformed and posts are formed by electrolytic plating. Finally, the resist is peeled off, the sputtered film is etched and the post-forming process is completed.

2. The mold die is divided into two pieces, an upper and a lower die. The lower die consists of inner and outer dies. These mold dies are heated to approximately 175 C and a temporary film is held by vacuum to upper die. The wafer on which the posts are formed is set on the inner die of the lower die and an encapsulant tablet is placed on the central part of the wafer with metal posts. The temporary film has three functions. To prevent the encapsulant from making contact with the upper die. 2) To disperse the mold pressure over the entire surface of the wafer. 3) To expose the top of the posts in the next stage. When clamping the mold die, the encapsulant tablet melts by applying heat and pressure. The encapsulant spreads over the entire wafer surface and hardens by held inside the mold die. Even though the encapsulant leaving out mold release agent and has an extremely high adhesive force, the encapsulated wafer can be released easily. This is because only a peripheral part of the mold die comes in contact with the encapsulant.

   Table 1 showed the reliability test results of a Cu post WLP package[6]. It clearly indicated that the reliability performance has been improved greatly.

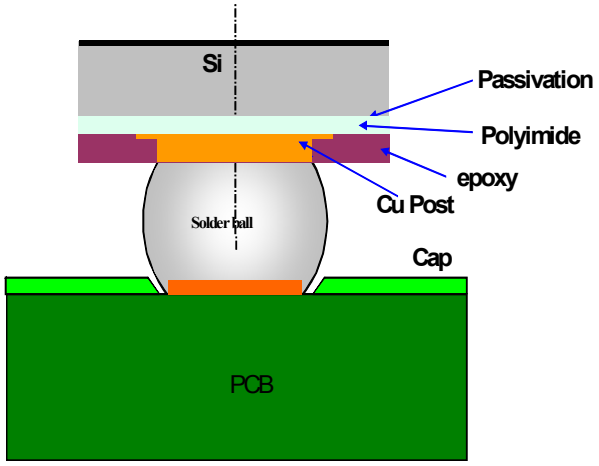

Fig. 2 A schematic of Cu post WLP structure

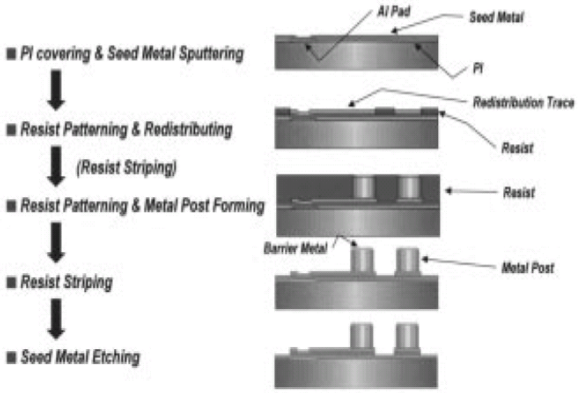

Fig. 3 Schematic diagrams of redistribution trace and metal post forming process.

Table 1 Cu post WLP package reliability

Test	Test Condition		Results
Temperature Cycle	-55/+125°C	N=20	1000cyc. PASS
Pressure Cooker	+121°C/85%RH	N=10	168Hrs PASS
Bending	Bending Span 3mm Bending Speed 5mm/min	N=10	OVER 15mm
Cyclic Bending	Bending Span 3mm	N=4	OVER 10000cyc.
Free fall			OVER 50cyc. OVER 2000cyc.

Bump on Polymer WLP

A typical structure for a bump on polymer (BOP) is shown in Fig. 4. In this structure the solder bump is placed over a layer of polymer dielectric material. There has been a strong performance driver for a WLP having a BOP structure. This technology minimizes the interconnect capacitance for high-speed application. In the case of a traditional BON structure (Fig. 1), the polymer is not subjected to stress originating in the solder bump since the solder bumps and UBM sits on silicon nitride. The typical failure mode has been ductile rupture through the solder at bump shear test and solder fatigue at temperature cycling (TC) tests. In the case of the

BOP WLPs, the bump rests on the polymer, and thus any stress applied to the solder bump directly propagates to the underlying polymer. The polymer must be designed to ensure sufficient mechanical toughness and adhesion to adjacent materials to qualify for the BOP structure.

The fabrication steps shown in Fig 5 follow the typical application steps used with photo definable polyimides [3]. The process is straightforward and requires two masks for opening vias in the dielectric layers and two masks for the metallization. The chosen polymer is photosensitive and positive acting, as are most photoresists in use today. Starting from a customer supplied wafer, a layer of polymer is applied over the existing passivation layer. The polymer thickness is targeted for 5 lm nominal after curing. The polymer precursor incorporates its own adhesion promoter, therefore saving an application and drying step. The material can be applied to any passivation material commonly used such as silicon dioxide, silicon nitride, silicon oxinitride, polyimide or similar classes of polymer that are less frequently used for passivation are equally acceptable.

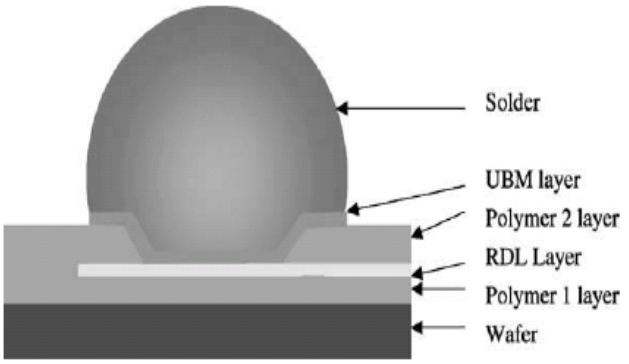

Fig. 4 a schematic of bump on polymer WLP

Because the photosensitizer used is closely related to common positive resists, the required exposure energy is similar to a thick photoresist. No incubation delay or other time constraint before development is necessary; the development can proceed immediately or a day or two later for convenience. The development proceeds in a manner similar to a positive photoresist, using either a puddle on a track system, or the old time honored technique of batch development in a bath, since no surface tension potential problem is expected from the large features prevailing in packaging. Partial curing of the polymer follows. Curing must be tightly controlled because the curing conditions affect the internal stresses and mechanical properties of polymers. A controlled atmosphere and controlled thermal cycle are recommended, even though this polymer is not subject to oxidation during curing and is thermooxidatively stable afterwards. Excellent planarization is obtained due to the high solid content of this material and low shrinkage. Partial curing is used to promote fusing of the subsequent polymer layer that will be applied on top, a technique developed in the 80┌s. The curing must be sufficient to eliminate any possibility of degassing during the following sputtering step and to provide sufficiently high stiffness to withstand the stresses imposed by the deposited metal layer.

At completion of the first layer curing, the redistribution metal layer can be sputtered over the bonding pads. In contrast to negative acting materials, no plasma etching of bond pads is necessary, since the polymer develops completely and very cleanly without leaving the usual residue in the center of the pad. This is partly due to better photosensitization and partly because the developer is a very slow etchant of aluminum. The developer is able to clean the pad after removing all the photosensitive material, leaving a fresh aluminum surface that later helps obtain a more reliable via contact.

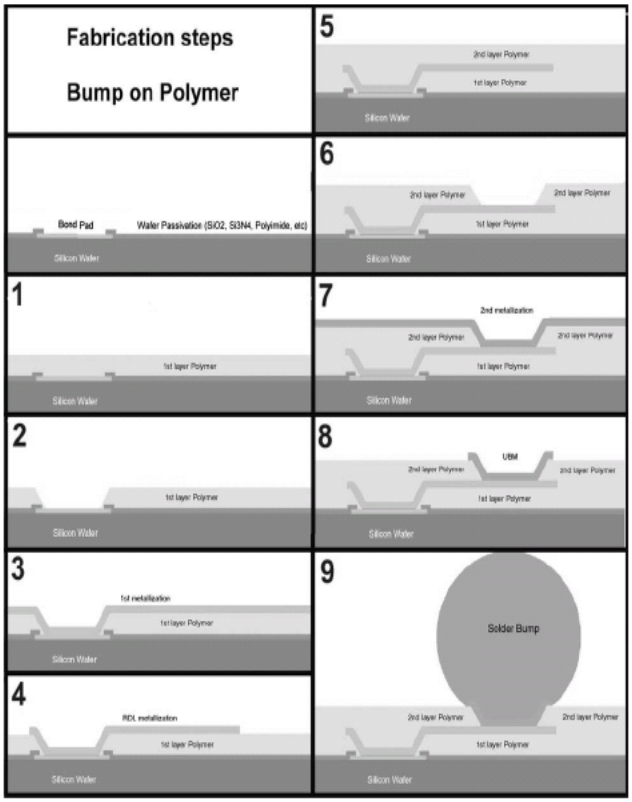

Fig. 5 Schematic of BOP WLP processes [3]

Two sets of TC tests have been carried out. CSP50 is a daisy chain test pattern having 0.5 mm pitch 10x10 array that was used for both test. In this test, the BOP structure consistently showed an approximate average 32% increase in Weibull life over the BON structure, as shown in Fig. 6.

There are a few different bump-on-polymer technologies and terminologies, as shown in Figs. 7-9, such as bump on RDL (Fig. 7), bump on thick repassivation/redistribution (Fig. 8), and bump on silicone bump (fig. 9).

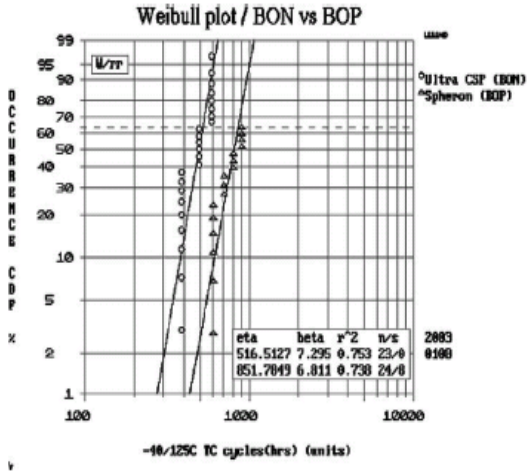

Fig. 6 Thermal cycling test results for BON vs. BOP

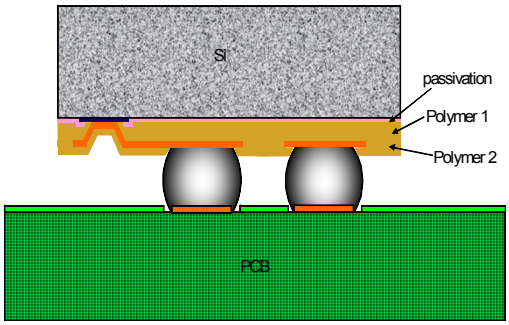

Fig. 7 Schematic of Bump on RDL

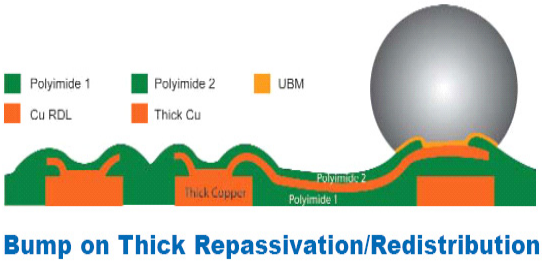

Fig. 8 Schematic of Bump on Repassivation/Redistribution

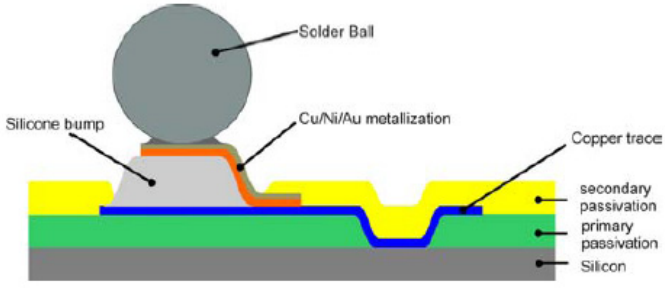

Fig. 9 Schematic of bump on silicone

Fan-Out or Redistributed Chip Packages (RCP) [7,8]

One of the most promising WLP technologies is the fan-out or redistributed chip packages (RCP). A schematic of such packages are shown in Figs. 10, and 11, respectively. Fig. 12 demonstrates the RCP process flow. Singulated die are placed with active side face-down on a substrate. The die are then encapsulated with a silica-filled epoxy molding compound. After cure, the panel of the die is then ground to the desired panel thickness and then released from the substrate. The die panelization process is done with standard assembly tools such as a pick and place tool. The epoxy panel with die then undergo a redistribution process to route out the signals, power, and ground. The redistribution process is done with standard silicon manufacturing equipment. These processing steps consist of the deposition of copper metallization layers by electroplating techniques. The metal layers are separated by insulating layers comprised of a spin-coated, photoimageable dielectric, and patterned using batch process lithography. The metal layers connect the pads on the die surface to the pads placed on the surface of the package, providing the same function as the metal layers in the substrate of a ball. grid array (BGA), but with a much finer resolution.

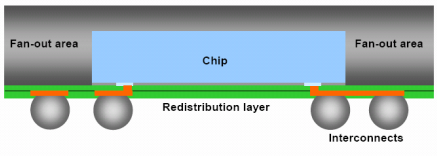

Fig. 10 Schematic of fan out packages

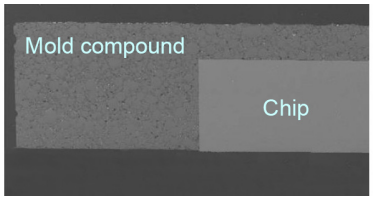

Fig. 11 molded die in a RCP package

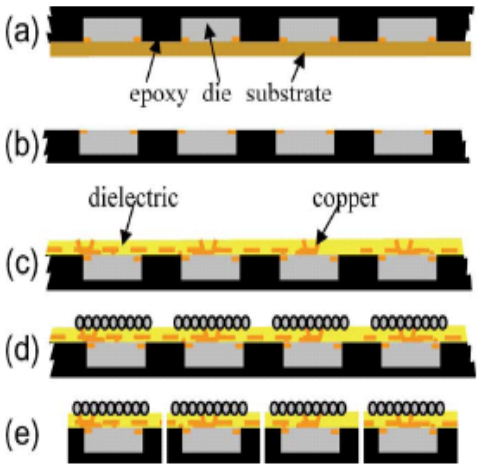

Fig. 12 RCP package process flow

Plastic Cored Solder Balls in WLPs

A plastic core solder ball consists of a large polymer core coated by a Cu layer and covered with eutectic and/or high melting SnPb solder. The main advantages of such a system are higher reliability due to the relaxing of stress by the polymer core and a defined ball height after reflow. These balls could be an alternative method as interconnection technique besides stencil printing and the use of preformed

full metallized solder balls. Fig. 13 shows the photos of the plastic core solder balls. Non-melting polymer-core copper and solder coated balls provide larger solder joint heights as well as more compliant 'solder balls' for greater reliability [14].

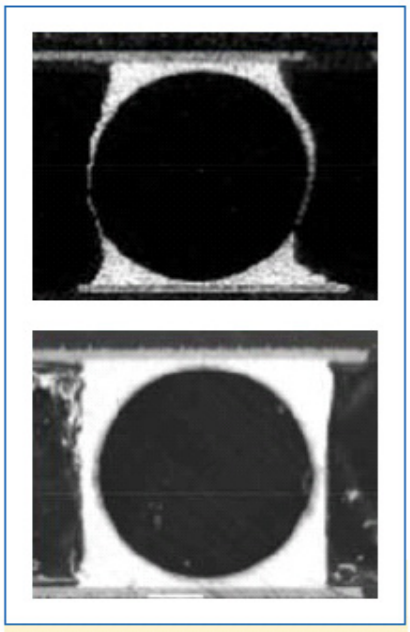

Fig. 13 microphotos of soler coated balls after reflow

Table 2 shows the plastic core material properties

Table 2. Some properties of the polymer cores of the 'SOL' balls.

Young's Modulus	4.9 GPa (-40 – 60°C) 4.7 GPa (60 – 200°C)
CTE	40.2 ppm/°C (-40 – 60°C) 46.2 ppm/°C (60 – 200°C)

Fig. 14 shows the comparison of the thermal cycling results [14]. It clearly indicates that the plastic core solder ball structures improve the fatigue life significantly. The Young's Modulus of plastic core is much smaller than that of metal, so it is superior in relaxing the thermal stress. The result of temperature cycle tests showed that it had excellent reliability and enabled much greater resistance to micro-cracks in the solder layer than that of conventional solder balls. In addition, it is superior in holding the gap flatly between upper and lower substrates, because the particle diameter of polymer core is very uniform.

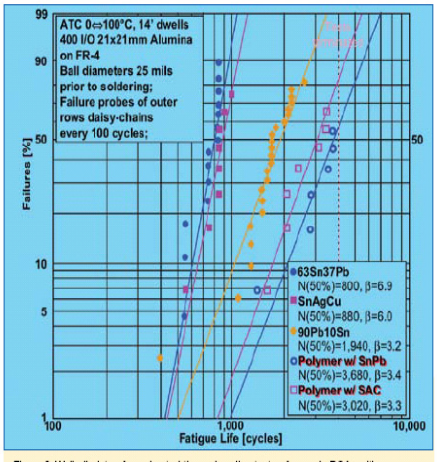

Fig. 14 Fatigue life comparison using plastic cored solder balls

Redistribution Applications in WLPs

Regardless of different classifications of the WLP technologies, redistribution becomes an essential part of each technology. Redistribution requires thin film polymers like secondary passivation and metallization to reroute the typical peripheral pad to an area array configuration. Redistribution technology not only realizes the rerouting, it also provides a mechanism for mechanical protection since such a layer acts as a stress buffer to release the stresses from solder joints. Similar ideas can be applied to the PCB side to enhance the WLP reliability.

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